

# Sam (Likun) Xi

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CONTACT INFORMATION	<b>Harvard University</b> School of Engineering and Applied Sciences Maxwell Dworkin, Room 307 33 Oxford Street Cambridge, MA 02138 USA	<i>Website:</i> <a href="http://www.samxi.org">www.samxi.org</a> <i>E-mail:</i> <a href="mailto:samxi@seas.harvard.edu">samxi@seas.harvard.edu</a>
RESEARCH INTERESTS	<b>Ccomputer architecture</b> , machine learning, deep neural networks, hardware accelerators, SoC design and integration, power and performance modeling, datacenter workloads.	
EDUCATION	<b>Harvard University</b> , Cambridge, MA 02138 S.M., Ph.D., <i>Computer Science</i> , August 2013 - Present · Advisors: David Brooks, Gu-Yeon Wei  <b>Duke University</b> , Durham, NC 27708 B.S.E, <i>Electrical and Computer Engineering</i> , May 2013 B.S., <i>Physics</i> , May 2013 · <i>Summa Cum Laude</i> , with Departmental Distinction · Final GPA: 3.937	
CONFERENCE PUBLICATIONS	Svilen Kanev, Sam (Likun) Xi, Gu-Yeon Wei, and David Brooks. “Mallacc: Accelerating Memory Allocation”, <i>Proc. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)</i> , April 2017. Best Paper Candidate.  Yakun Sophia Shao, Sam (Likun) Xi, Viji Srinivasan, Gu-Yeon Wei, and David Brooks. “Co-Designing Accelerators and SoC Interfaces Using gem5-Aladdin”, <i>Proc. International Symposium on Microarchitecture (MICRO)</i> , October 2016.  Sam (Likun) Xi, Oreoluwa Babarinsa, Manos Athanassoulis, and Stratos Idreos. “Beyond the Wall: Near-Data Processing for Databases”, <i>SIGMOD Workshop on Data Management on New Hardware (DaMoN)</i> , June 2015.  Sam (Likun) Xi, Hans Jacobson, Pradip Bose, Gu-Yeon Wei, and David Brooks. “Quantifying Sources of Error in McPAT and Potential Impacts on Architectural Studies”, <i>Proc. International Symposium on High Performance Computer Architecture (HPCA)</i> , February 2015.  Yakun Sophia Shao, Sam Xi, Viji Srinivasan, Gu-Yeon Wei, and David Brooks. “Towards Cache-Friendly Hardware Accelerators”, <i>In Sensors and Cloud Architectures Workshop, High Performance Computer Architecture (HPCA)</i> , February 2015.  Sam Xi, Marisabel Guevara, Jared Nelson, Patrick Pensabene, and Benjamin C. Lee. “Understanding the Critical Path in Power State Transition Latencies”, <i>Proc. International Symposium on Low Power Electronics and Design (ISLPED)</i> , September 2013.	
PROFESSIONAL EXPERIENCE	<b>NVIDIA Corporation</b> , Architecture Research Group, Westford, MA 01886 <i>Research Intern</i>	<b>May 2017 to August 2017</b> · Supervisor: Joel Emer, Steve Keckler · Evaluated the tradeoffs of building flexible machine learning hardware accelerators. · Implemented sparse convolution on a prototype DNN accelerator in synthesizable SystemC to evaluate its performance on a new workload.

- Implemented various dense convolutional dataflows on this prototype to compare its performance against fixed-function accelerators.

**NVIDIA Corporation**, ASIC/VLSI Research Group, Santa Clara, CA 95050

*Research Intern*

**May 2015 to August 2015**

- Supervisor: Brucek Khailany
- Investigated using high-level synthesis tools to supplant hand-written RTL for hardware prototyping and design in a commercial setting.
- Implemented various parameterizable floating-point units in C++ using HLS tools.
- Implemented the texture filtering stage from Pascal GPU using HLS and obtained comparable quality-of-result compared to hand-written RTL.
- Implemented synthesizable cache simulator in SystemC for use in rapid prototyping of new hardware designs.

**Google Inc.**, Ads Backend, Mountain View, CA 94043

*Software Engineering Intern*

**May 2013 to August 2013**

- Supervisor: Jojo Dijamco
- Implemented components of a new frontend for a big data analytics platform.
- Implemented a new tool to parse source code comments for presentation to end users.
- Investigated a new backend server architecture to speed up development and push cycles and improve collaboration among different teams working on the same product.

**Google Inc.**, YouTube Data Analytics, Mountain View, CA 94043

*Software Engineering Intern*

**May 2012 to August 2012**

- Supervisor: Neil McKay
- Rebuilt internal dashboards for monitoring of logs analysis jobs from ground up, without any reliance on an intermediary presentation layer.
- Integrated multiple internal dashboards into a unified user interface.

**AWARDS**

**Harvard University**

- Gordon McKay Graduate Research Fellowship, 2013.
- James Mills Peirce Fellowship, 2013

**National Science Foundation**

- Graduate Research Fellowship, 2013 - 2016.

**Duke University**

- Charles Ernest Seager Memorial Award, 2013
- ECE Department, Best Poster Award, 2013.
- Top 5% of 2013 Engineering Class.
- Dean's List with Distinction 2009-2013.

**Honors Societies**

- Phi Beta Kappa Honors Society.
- Sigma Pi Sigma Physics Society.
- Tau Beta Pi Engineering Society.

**SKILLS**

**Programming**

- Languages: C, C++, Python, Java, SystemC
- OS: Experience with the Linux kernel on both x86 and ARM
- CAD tools: Catapult HLS, Vivado Design Suite

**I am the primary maintainer of:**

- gem5-Aladdin, an SoC simulator  
<https://github.com/harvard-acc/gem5-aladdin>
- Aladdin, an accelerator power/performance/area simulator  
<https://github.com/ysshao/Aladdin>
- LLVM-Tracer, an LLVM optimization pass used by Aladdin  
<https://github.com/ysshao/LLVM-Tracer>

REFERENCES

**Dr. David Brooks** (dbrooks@eecs.harvard.edu; (617) 495-3989)

- Haley Family Professor of Computer Science
- School of Engineering and Applied Sciences, Harvard University.

**Dr. Gu-Yeon Wei** (guyeon@eecs.harvard.edu; (617) 495-3989)

- Gordon McKay Professor of Electrical Engineering
- School of Engineering and Applied Sciences, Harvard University.

**Dr. Michael Pellauer** (mpellauer@nvidia.com)

- Senior Research Scientist.
- Architecture Research Group, NVIDIA.